CSC 211.02 **Assignment 5: Performance** **Fall 2015**

Assigned: Thursday 1 October

Due: Wednesday 7 October 10:30 pm

Collaboration: This assignment must be completed individually.

Presentation: Complete sentences should explain all steps in deriving final answers.

Submission: Upload a PDF with your name, box number, and all solutions to PioneerWeb.

Problem 1: System requirements and capabilities

A standard resolution for digital video is 2048×1080 pixels per frame. Each pixel is represented in the CIE XYZ color space using 12 bits per component, or 36 bits per pixel. A standard frame rate is 24 frames per second.

a) How much memory is required to store a single frame of video in this format?

b) How much memory is required to store one second of data?

c) How much memory is required to store a two hour movie?

d) If a server is connected to 1 Gbps Ethernet (1 Gbps = 1 billion bits per second), how many frames per second can it stream? *You may assume that 100% of the network bandwidth (without overhead) is available to transmit the video.*

Give your answers in the most sensible units.[1]

Problem 2: Instruction mix

Suppose a 3.75 GHz processor has four classes of instructions: Compute, Load, Store, and Branch. The following table shows the number of cycles required to execute each class of instruction, as well as the number of instructions of each type executed by a particular program.

	Compute	**Load**	**Store**	**Branch**
Cycles	1	4	5	2
IC	600	100	75	20

a) How long does it take to run this program on this processor?

b) What is the overall CPI for the program?

c) If a clever programmer can cut the number of load instructions in half, by what factor would performance improve?

Problem 3: Performance fallacies

This problem investigates three common performance fallacies:

- Faster clock speed means better performance.
- More instructions means more time.
- Higher MIPS (millions of instructions per second) means better performance.

Consider the following data for the execution of a given sequence of one million instructions on two different processors implementing the same instruction set architecture.

[1] For example, giving the distance between Grinnell and Des Moines as 3,364,416 inches is not sensible. Neither is reporting that distance as 0.000000000009033 light years.

CPU	Freq	CPI
A	4 GHz	1.25
B	3 GHz	0.75

a) Determine the performance of both processors. Does faster clock rate mean better performance?

b) How many instructions can CPU B run in the time it takes CPU A to run a million instructions? Does executing more instructions necessarily take more time?

c) Compute the MIPS for both processors. Does higher MIPS mean better performance?

Problem 4: Multicore power versus speedup

Suppose that a given program can be parallelized to run on 1, 2, 4, or 8 cores, but running the program in parallel requires additional instructions to coordinate across cores. The table below shows the number of instructions that must be executed on each core for a given number of cores.

Cores	IC/core
1	1×10^{10}
2	6×10^{9}
4	4×10^{9}
8	3×10^{9}

a) Assuming a 4 GHz clock and a CPI of 1.2, what is the program execution time in each scenario?

b) Recall that the power consumption of a processor core is

$$P = C \times V^2 \times f, \tag{1}$$

where P is power in Watts, C is capacitance in Farads, V is voltage in Volts, and f is frequency in Hertz. Assume that each core runs at 3 GHz with a capacitance of 2×10^{-9} Farads at 1.75 Volts. Find the cumulative power consumption of the program in each scenario.

c) What is the program execution time and power consumption in each scenario if we "downgrade" the system to 2 GHz cores, assuming the voltage and capacitance remain the same (an unlikely scenario).

Problem 5: Parallelism versus clock speed

Nearly all power consumed by a processor is turned into heat, also measured in Watts. The physical size of the processor and its heat sink determines the rate at which this heat can be dissipated (called the thermal design power or *TDP*. According to Equation (1), increasing frequency increases power consumption and therefore heat output.

The Intel Xeon E5-2640 v3 processor has eight cores, a TDP of 90 W, and operates at 2.6 GHz.[2] This processor has a feature allowing it to run at higher clock speeds when some cores are inactive, as long as the total power consumption is below the TDP.

a) If we assume an idle core consumes no power, what clock frequencies could this processor support with just one, two, or four active cores? Assume that the processor consumes exactly 90 W when running at 2.6GHz with all eight cores active.

b) The maximum frequency for this processor is actually 3.2 GHz with just one core enabled. Thus idle cores must consume *some* power. Determine the power consumption of active and idle cores at 2.6 GHz. Remember to account for the increased power consumption of both active and idle cores when the processor is running at a higher frequency. Assume all cores run at the same frequency.

Acknowledgments This derivative work of Janet Davis, used under the Creative Commons Attribution-Noncommercial-Share Alike 3.0 United States License was developed in collaboration with Charlie Curtsinger. Problems 1–4 are adapted from Patterson & Hennessy (2008), Exercises 1.2, 1.5, 1.3, and 1.10 (pp. 58–67).[3]

[2] Intel (n.d.) Intel® Xeon® Processor E5-2640 v3 (20M Cache, 2.60 GHz). http://ark.intel.com/products/83359

[3] Patterson, D. A., & Hennessy, J. L. (2008). *Computer organization and design: The hardware/software interface* (Fourth Edition). Morgan Kaufmann: Burlington, MA.